WHAT IS CLAIMED IS:

1. A data processing apparatus comprising:

an operation processing unit having at least a read cycle period when said operation processing unit reads data from a device, and a write cycle period when said operation processing unit writes data in the device;

a memory which performs data transmission/ reception between said operation processing unit and said memory;

a data bus connected to said operation processing unit and said memory; and

a pseudo-data generating circuit connected to said data bus, said pseudo-data generating circuit which generates pseudo-data and outputs the pseudo-data to said data bus in a time interval between the read cycle period and the write cycle period, between the write cycle period and the read cycle period, between two read cycle periods, or between two write cycle periods.

2. The data processing apparatus according to claim 1, wherein said pseudo-data generating circuit generates random number data as the pseudo-data.

3. A data processing apparatus comprising:

an operation processing unit which performs operation processing;

a memory which performs data transmission/ reception between said operation processing unit and

said memory;

a data bus connected to said operation processing unit and said memory;

a read signal line and a write signal line connected to said operation processing unit and said memory;

a control signal generating circuit connected to said read signal line and said write signal line, said control signal generating circuit detects a change in a read control signal and a write control signal transmitted to said read signal line and said write signal line, respectively, and then generates a control signal; and

a pseudo-data generating circuit connected to said control signal generating circuit so as to receive the control signal and connected to said data bus, said pseudo-data generating circuit generates pseudo-data and outputs the pseudo-data to said data bus in accordance with the control signal.

4. The data processing apparatus according to claim 3, wherein said pseudo-data generating circuit generates random number data as the pseudo-data.

5. A data processing apparatus comprising:

an operation processing unit having at least a read cycle period when said operation processing unit reads data from a device, and a write cycle period when said operation processing unit writes data in the

device;

a memory which performs data transmission/ reception between said operation processing unit and said memory;

a data bus connected to said operation processing unit and said memory; and

a dummy circuit connected to said data bus, said dummy circuit operates and consumes power in a time interval between the read cycle period and the write cycle period, between the write cycle period and the read cycle period, between two read cycle periods, or between two write cycle periods.

6. The data processing apparatus according to claim 5, wherein said dummy circuit is a counter circuit.

7. The data processing apparatus according to claim 5, wherein said dummy circuit is a shift register circuit.

8. A data processing apparatus comprising:

an operation processing unit which performs operation processing;

a memory which performs data transmission/ reception between said operation processing unit and said memory;

a data bus connected to said operation processing unit and said memory;

a read signal line and a write signal line

connected to said operation processing unit and said memory;

a control signal generating circuit connected to said read signal line and said write signal line, said control signal generating circuit detects a change in a read control signal and a write control signal transmitted to said read signal line and said write signal line, respectively, and then generates a control signal; and

a dummy circuit connected to said control signal generating circuit so as to receive the control signal and connected to said data bus, said dummy circuit operates and consumes power in accordance with the control signal.

9. The data processing apparatus according to claim 8, wherein said dummy circuit is a counter circuit.

10. The data processing apparatus according to claim 8, wherein said dummy circuit is a shift register circuit.

11. A memory card comprising:

an operation processing unit having at least a read cycle period when said operation processing unit reads data from a device, and a write cycle period when said operation processing unit writes data in the device;

a memory which performs data

transmission/reception between said operation processing unit and said memory;

a data bus connected to said operation processing unit and said memory;

an input/output circuit connected to said data bus, said input/output circuit outputs external data onto said data bus and outputs data on said data bus to an external apparatus; and

a pseudo-data generating circuit connected to said data bus, said pseudo-data generating circuit generates pseudo-data and outputs the pseudo-data to said data bus in a time interval between the read cycle period and the write cycle period, between the write cycle period and the read cycle period, between two read cycle periods, or between two write cycle periods.

12. The memory card according to claim 11, wherein said pseudo-data generating circuit generates random number data as the pseudo-data.

13. A memory card comprising:

an operation processing unit which performs operation processing;

a memory which performs data transmission/ reception between said operation processing unit and said memory;

a data bus connected to said operation processing unit and said memory;

an input/output circuit connected to said data

bus, said input/output circuit outputs external data onto said data bus and outputs data on said data bus to an external apparatus;

a read signal line and a write signal line connected to said operation processing unit and said memory;

a control signal generating circuit connected to said read signal line and said write signal line, said control signal generating circuit detects a change in a read control signal and a write control signal transmitted to said read signal line and said write signal line, respectively, and then generates a control signal; and

a pseudo-data generating circuit connected to said control signal generating circuit so as to receive the control signal and connected to said data bus, said pseudo-data generating circuit generates pseudo-data and outputs the pseudo-data to said data bus in accordance with the control signal.

14. The memory card according to claim 13, wherein said pseudo-data generating circuit generates random number data as the pseudo-data.

15. A memory card comprising:

an operation processing unit having at least a read cycle period when said operation processing unit reads data from a device, and a write cycle period when said operation processing unit writes data in the

device;

a memory which performs data transmission/ reception between said operation processing unit and said memory;

a data bus connected to said operation processing unit and said memory;

an input/output circuit connected to said data bus, said input/output circuit outputs external data onto said data bus and outputs data on said data bus to an external apparatus; and

a dummy circuit connected to said data bus, said dummy circuit operates and consumes power in a time interval between the read cycle period and the write cycle period, between the write cycle period and the read cycle period, between two read cycle periods, or between two write cycle periods.

16. The memory card according to claim 15, wherein said dummy circuit is a counter circuit.

17. The memory card according to claim 15, wherein said dummy circuit is a shift register circuit.

18. A memory card comprising:

an operation processing unit which performs operation processing;

a memory which performs data transmission/ reception between said operation processing unit and said memory;

a data bus connected to said operation processing

unit and said memory;

an input/output circuit connected to said data bus, said input/output circuit outputs external data onto said data bus and outputs data on said data bus to an external apparatus;

a read signal line and a write signal line connected to said operation processing unit and said memory;

a control signal generating circuit connected to said read signal line and said write signal line, said control signal generating circuit detects a change in a read control signal and a write control signal transmitted to said read signal line and said write signal line, respectively, and then generates a control signal; and

a dummy circuit connected to said control signal generating circuit so as to receive the control signal and connected to said data bus, said dummy circuit operates and consumes power in accordance with the control signal.

19. The memory card according to claim 18, wherein said dummy circuit is a counter circuit.

20. The memory card according to claim 18, wherein said dummy circuit is a shift register circuit.